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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,267	09/26/2001	Haruo Hyodo	10417-101001	8383

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,267	HYODO ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-13* is/are pending in the application.

4a) Of the above claim(s) *4-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Applicants' amendment filed March 26, 2003.

Specification

The objection to the title of the invention has been withdrawn due to the amendment filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 8-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 9A-9B in view of Ozimek et al. (5,382,310), Toshiba KK [Toke] (JP07225391A), Hirose et al. (5,898,218) and Sasano (US 6,313,525 B1).

Admitted Prior Art Figures 9A-9B teach a semiconductor device comprising: a supporting substrate **1** made of insulating material; three conductive patterns provided on a surface of the supporting substrate; an external connecting terminal **2** electrically connected to the conductive patterns; a semiconductor circuit element **5**; and a ceramic plate **3** that covers the circuit element and that forms a hollow airtight portion **7** between

the supporting substrate and the ceramic plate. However, Admitted Prior Art Figures 9A-9B fail to teach a glass plate, an external connecting terminal provided on a back surface of the supporting substrate electrically connected to the conductive pattern through the substrate by a via hole, and a light-shielding adhesive resin applied over an entire surface of the glass plate. Prior Art Figures 9A-9B further teach an insulating substrate **1**. Ozimek et al. teach an adhesive **26** applied over an entire surface of the glass plate **28** (Figure 1, col. 3, lines 9-31). Toshiba KK [Toke] teaches a light-shielding adhesive resin. Hirose et al. teach an external connecting terminal 14 provided on a back surface of the supporting substrate 10 electrically connected to the conductive pattern through the substrate by a via hole 13 (Figure 1, col. 4, lines 16-59). Sasano teaches a glass plate **9** with an adhesive resin **10** applied over a surface of the glass plate and an external connecting terminal **6** provided on a back surface of the supporting substrate (Figure 1, column 6, lines 6-10). Sasano further teach a wall surrounding the circuit member **7-8**, wherein the transparent plate **9** adhered on the wall over the circuit member **7-8** to form an airtight cavity between the substrate **1** and the transparent plate **9** (Figure 1) and a semiconductor chip 7 disposed over the conductive pattern which is disposed over the substrate. Since Admitted Prior Art Figures 9A-9B, Ozimek et al., Toshiba KK [Toke], Hirose et al. and Sasano are from the same field of endeavor (semiconductor devices), the purpose disclosed by Sasano would have been recognized in the pertinent art of Admitted Prior Art Figures 9A-9B, Ozimek et al., Toshiba KK [Toke] and Hirose et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the

semiconductor device of Admitted Prior Art Figures 9A-9B by incorporating the adhesive of Ozimek et al., the light-shielding adhesive resin of Toshiba KK [Toke], the via hole of Hirose et al. and the glass plate, adhesive resin and external connection of Sasano to maintain air tightness (col. 3, lines 12-21).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figures 9A-9B, Ozimek et al. (5,382,310), Toshiba KK [Toke] (JP07225391A), Hirose et al. (5,898,218) and Sasano (US 6,313,525 B1) as applied to claims 1, 3, 8-10 and 12-13 above, and further in view of Kuriyama (5,682,057).

Prior Art Figures 9A-9B, Ozimek et al., Toshiba KK [Toke] (JP07225391A), Hirose et al. and Sasano teach all mentioned in the rejection above. However, Prior Art Figures 9A-9B, Ozimek et al., Toshiba KK [Toke], Hirose et al. and Sasano fail to teach a fuse element. Kuriyama teaches a fuse element 7 (Figure 1, col. 3, lines 4-67). Since Admitted Prior Art Figures 9A-9B, Ozimek et al., Toshiba KK [Toke], Hirose et al., Sasano and Kuriyama are from the same field of endeavor (semiconductor devices), the purpose disclosed by Kuriyama would have been recognized in the pertinent art of Admitted Prior Art Figures 9A-9B, Ozimek et al., Toshiba KK [Toke], Hirose et al. and Sasano. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Admitted Prior Art Figures 9A-9B, the adhesive of Ozimek et al., the light-shielding adhesive resin of Toshiba KK [Toke], the via hole of Hirose et al. and the glass plate, adhesive resin and

external connection of Sasano by incorporating the fuse element of Kuriyama to avoid extensive damage when exposed to excessive temperature rise (col. 1, lines 7-10).

Response to Arguments

Applicant's arguments with respect to Hyoudo et al. (US 6,365,433 B1) have been considered but are moot in view of the newly applied reference. Applicant's arguments with respect to the remaining referenced have been fully considered but are not persuasive. In response to applicant's argument that Toshiba, Sasano and Ozimek are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Toshiba, Sasano and Ozimek are all semiconductor structures.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to semiconductor devices having fuse elements:

Kalnitsky et al. (US 6,525,397 B1) Kawauchi (5,277,356)

Whitney (US 6,507264 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
October 16, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800